

REMARKS

At the outset, the Examiner is thanked for the thorough review and consideration of the pending application. The Office Action dated November 15, 2007, has been received and its contents carefully reviewed.

Claims 1, 3, 5, 7-12, 14-30, 32, and 34-47 are rejected by the Examiner. With this response, claims 1, 9, 11, and 35 have been amended. Claim 10 is canceled without prejudice or disclaimer. No new matter has been added. Claims 1, 3, 5, 7-9, 11, 12, 14-30, 32, and 34-47 remain pending in this application.

In the Office Action, claims 1, 3, 5, 7-12, 14-30, 32, and 34-47 are rejected under 35 U.S.C. § 112, first paragraph as failing to comply with the written description requirement. Claims 1, 5, 7, 8, 30, and 34 are rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Publication No. 2002/0030653 to Cairns et al. (hereinafter "Cairns1") in view of U.S. Patent No. 6,268,841 to Cairns et al. (hereinafter "Cairns2") and further in view of U.S. Patent No. 5,892,493 to Enami et al. (hereinafter "Enami"). Claims 3 and 32 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Cairns1 and Cairns2 in view of Nitta. Claims 9-12, 14-29, and 35-47 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Cairns1 in view of Cairns2, Enami, and Nitta.

Rejection of claims under 35 U.S.C. § 112, first paragraph

The rejection of claims 1, 3, 5, 7-12, 14-30, 32, and 34-47 under 35 U.S.C. § 112, first paragraph as failing to comply with the written description requirement is respectfully traversed and reconsideration is requested.

With respect to the rejection to claim 1, the Office Action indicates that claim 1 recites "a second multiplexer part providing the corresponding data lines with the pixel signals from the output buffer part (lines 14-15)," and indicates that there is no support in the specification for this feature in combination with "an output part outputting simultaneously the analog pixel signals from the corresponding demultiplexer output channels to corresponding data lines (lines 8-9)." which the examiner associates with the third embodiment.

Applicants respectfully disagree with the examiner's conclusion. More completely, claim 1 recites "a second multiplexer part providing the corresponding data lines with the pixel signals from the output buffer part for the enable period of a source output enable signal and a reference voltage of liquid crystal cells for the disabled period of the source output enable signal." Applicants submit that a multiplexer functioning as described above is described in combination

with multiple embodiments disclosed in the specification. For example, Figure 7 shows a multiplexer part 276, and paragraph [0130] of Applicants' Specification states the following:

"The MUX3 part 276 is connected between the output buffer part 274 and the data lines and controls the supplying timing of the pixel signals in response to the MSOE signal shown in FIG. 8. More specifically, the MUX3 part 276 supplies the pixel signals from the output buffer part 274 to the data lines DL1 to DL4 for the enable period of the MSOE signal shown in FIG. 8 and supplies the common voltage to each of the data lines DL1 to DL4 for the disable period."

Similar multiplexers in connection with other embodiments of the invention are described at least at paragraphs [0058] and [0125]. Applicants submit that the combination of features recited in claim 1 fully complies with the written description requirement of 35 U.S.C. § 112, first paragraph.

With respect to the rejection to claim 3, item 4 of the Office Action indicates that claim 3 is being interpreted as describing the embodiment shown in Fig. 3, and states, "there is no support in the drawings nor the specifications for a third multiplexer." As Applicants have discussed above, the features identified by the Examiner in claim 1 do not identify claim 1 as covering the embodiment pictured in Fig. 3. Accordingly, Applicants submit that the combination of features recited in claim 3 is fully supported by Applicants' Specification.

With respect to independent claims 9, 30, and 35, the Office Action does not explicitly discuss the limitations of these claims, and relies on the discussion of the rejection of claim 1. Applicants note that claims 9, 30, and 35 do not recite the combination of features identified in the Office Action as lacking support. For example, claim 9 does not recite "a second multiplexer part providing the corresponding data lines with the pixel signals from the output buffer part". Accordingly, the rejection applied in claim 1 would not apply to claims 9, 30, and 35. Further, the combination of features recited in claim 1 is supported by Applicants' specification as discussed above. Accordingly, Applicants respectfully submit that claims 9, 30, and 35 fully comply with the written description requirement of 35 U.S.C. § 112, first paragraph.

As the rejections of the dependent claims are based on their dependencies from claims 1, 9, 30 and 35, Applicants respectfully request that the rejections to claims 1, 3, 5, 7-12, 14-30, 32, and 34-47 under 35 U.S.C. § 112, first paragraph as failing to comply with the written description requirement be withdrawn for the reasons given above.

Rejection of claims under 35 U.S.C. § 103(a)

The rejection of claims 1, 5, 7, 8, 30, 34, and 35 under 35 U.S.C. § 103(a) as being unpatentable over Cairns1 and Cairns2, in view of Enami are respectfully traversed and reconsideration is requested.

Independent claim 1 recites a data driving apparatus for a liquid crystal display device having a combination of features including, for example, “a second multiplexer part providing the corresponding data lines with the pixel signals from the output buffer part for the enable period of a source output enable signal and a reference voltage of liquid crystal cells for the disabled period of the source output enable signal.” Applicants submit that Cairns1, Cairns2, and Enami, analyzed singly or in any combination do not teach or suggest at least this combination of features recited in claim 1.

In the Office Action, it is alleged that that Fig. 2 of Cairns1 discloses “providing the corresponding data lines with the pixel signals from the output buffer part for the enable period of a source output enable signal and a reference voltage of liquid crystal cells for the disabled period of the source output enable signal.”

Applicants respectfully disagree with the Examiner’s conclusion regarding the teachings of Cairns1. No portion of Cairns1, including Fig. 2 cited in the Office Action discloses “a second multiplexer part providing the corresponding data lines with ... a reference voltage of liquid crystal cells for the disabled period of the source output enable signal.”

Applicants further submit that Cairns2 and Enami do not teach at least this feature of the claims.

With respect to the argument in Applicants previous response filed on September 28, 2007 that Cairns1, Cairns2, and Enami do not teach the above cited combination of features of claim 1, the ‘Response to Arguments’ of the Office Action, indicates Applicants’ argument is not persuasive because “There is not support for this newly added claim language.”

First, As Applicants have discussed above, Applicants’ specification describes a multiplexer “part providing the corresponding data lines with the pixel signals from the output buffer part for the enable period of a source output enable signal and a reference voltage of liquid crystal cells for the disabled period of the source output enable signal” for multiple embodiments including the embodiments shown in Figs. 3 and 7 of Applicants’ specification, with the labeling of this multiplexer as “second” or “third” being of no consequence.

Secondly, even were the Examiner correct concerning the lack of support for the claimed combination of features, a proper rejection under 35 U.S.C. §103(a) would include consideration of even allegedly unsupported claim features. M.P.E.P. 2143.03 states, “When evaluating claims for obviousness under 35 U.S.C. 103, all the limitations of the claims must be considered and given weight, including limitations which do not find support in the specification as originally filed ...” Accordingly, Applicants respectfully request that the rejection to claim 1 under 35 U.S.C. §103(a) be withdrawn as the cited references, analyzed singly or in any combination, do not teach or suggest all of the features of claim 1.

Claim 1 further recites “a demultiplexer part separately supplying the analog pixel signals from the digital-analog converter part to a plurality of output channels, respectively during the first half of a horizontal period and during the second half of the horizontal period.” Applicants submit that claim 1 is allowable over the cited references for the additional reason that Cairns1, Cairns2, and Enami, analyzed singly or in any combination, do not teach or suggest this additional combination of features recited by claim 1.

Claims 5, 7, and 8 depend from claim 1 and include by reference all of the features recited in claim 1. Applicants submit that claims 5, 7, and 8 are each allowable over the cited references at least based on their dependencies and for the same reasons given for claim 1.

Claims 30 and 34 each recites a data driving method for a liquid crystal display device having a combination of features including “providing the corresponding data lines with the held pixel signals for an enable period of an input source output enable signal and a reference voltage of liquid crystal cells for a disable period of the input source output enable signal.”

Applicants submit that the Cairns1, Cairns2, and Enami, do not teach or suggest at least this combination of features. For example, there is no teaching of “providing the corresponding data lines with ... a reference voltage of liquid crystal cells for a disable period of the input source output enable signal.” Accordingly, Applicants respectfully submit that claims 30 and 34 are allowable over Cairns1, Cairns2, and Enami.

The rejection of claims 3 and 32 under 35 U.S.C. § 103(a) as being unpatentable over Cairns1 and Cairns2, in view of Nitta is respectfully traversed and reconsideration is requested.

As an initial matter, Applicants note that claims 3 and 32 each depend respectively from claims 1 and 30, and that each includes by reference all of the features of its respective base claim.

As discussed above, Cairns1, Cairns2, and Enami do not teach or suggest at least “providing the corresponding data lines with the held pixel signals for an enable period of an input source output enable signal and a reference voltage of liquid crystal cells for a disable period of the input source output enable signal” as recited in claims 1 and 30. The Examiner cites Nitta as teaching “a positive digital-analog converter converting the digital pixel data to a positive pixel signal; a negative digital-analog converter converting the digital pixel data to a negative pixel signal in accordance with a polarity control signal.” Applicants do not reach the Examiner’s conclusion regarding the teachings of Nitta. Applicants submit that Nitta does not cure the deficiencies in the teachings of Cairns1, Cairns2, and Enami with respect to the combined features recited in claims 1 and 30 as discussed above. Accordingly, Applicants submit that the Examiner has failed to establish a prima facie case of obviousness of claim 1 and 30, and claims 3 and 32 depending respectively from claims 1 and 30 over Cairns1, Cairns2, Enami and Nitta.

The rejection of claims 9, 11, 12, 14-29, 35-47 under 35 U.S.C. 103(a) as being unpatentable over Cairns1 in view of Cairns2, Enami, and Nitta is respectfully traversed and reconsideration is required.

Claim 9 recites a data driving apparatus for a liquid crystal display device having a combination of features including “a multiplexer part performing a time-division on inputted digital pixel data on a first horizontal period and providing the time-divided pixel data through positive and negative polarity output channels; a digital-analog converter part converting the time-divided digital pixel data received from each of the multiplexer output channels into time-divided analog pixel signals having a polarity corresponding to the polarity of the respective multiplexer output channel; a demultiplexer part providing the time-divided pixel signal received from the digital-analog converter to output channels of the demultiplexer corresponding to the data lines” Applicants submit that Cairns1, Cairns2, Enami, and Nitta, analyzed singly or in any combination, do not each at least the above-identified combination of features recited in claim 9.

Cairns1, Cairns2, and Enami do not teach using “a digital-analog converter part including: a positive digital-analog converter ... and a negative digital-analog converter” in any configuration. Accordingly, these references, analyzed singly or in combination fail to teach or suggest “a positive digital-analog converter converting a plurality of time divided pixel data for the first horizontal period provided through the positive polarity output channel of the multiplexer part into positive pixel data; and a negative digital-analog converter converting a

plurality of time divided pixel data for the first horizontal period provided through the negative polarity output channel of the multiplexer part into negative pixel data” at least because the references do not suggest “a positive polarity output channel and a negative polarity output channel” as recited in claim 9.

In the Office Action, Nitta is cited as curing the deficiencies in the teachings of Cairns1, Cairns2, and Enami. In particular, the Office Action states, “Nitta teaches of the components of the driving apparatus having selected polarity via positive and negative polarity output channels/paths (column 3, lines 23-33, column 4, lines 25-30).” See Office Action page 9, last sentence. Applicants respectfully disagree that Nitta, including the portions cited by the Examiner, cures the deficiencies in Cairns1, Cairns2, and Enami noted above.

As shown in Figs. 2, 4, and 7, Nitta, alone or in any combination with Cairns1, Cairns2, and Enami does not teach or suggest at least “a positive digital-analog converter converting a plurality of time divided pixel data for the first horizontal period provided through the positive polarity output channel of the multiplexer part into positive pixel data” because Nitta does not teach or suggest a positive digital to analog converter “converting a plurality of time divided pixel data for the first horizontal period.” For example, regarding the circuit of Fig. 2, Nitta states the following at column 4, lines 20-25:

“One line of data, once acquired, is latched by the horizontal latch signal 220 to the latch circuit 222, one line at a time, during the horizontal period. The selection circuit 226 selects the display data of two pixels corresponding to the neighboring output in accordance with the alternately switching timing. The DAC circuit 228 generates the positive-polarity gray-scale voltage, while the DAC circuit 229 generates the negative-polarity gray-scale voltage. Therefore, the selection circuit 226 selects display data depending upon whether the neighboring output is in the positive polarity or negative polarity.”

Applicants submit that Nitta discloses that a positive DAC that outputs a single positive voltage for a horizontal period and not “converting a plurality of time divided pixel data for the first horizontal period provided through the positive polarity output channel of the multiplexer part” as recited in claim 9.

Similarly, Nitta does not teach or suggest “a negative digital-analog converter converting a plurality of time divided pixel data for the first horizontal period provided through the negative polarity output channel of the multiplexer part into negative pixel data.” Accordingly, Applicants submit that Nitta fails to cure the identified deficiencies in the teachings of Cairns1, Cairns2, and Enami. Applicants submit that Cairns1, Cairns2, Enami, and Nitta, analyzed singly

or in combination, do not teach or suggest the combined features of claim 9, and that claim 9 is allowable over Cairns1, Cairns2, Enami, and Nitta for at least the reasons discussed above.

Claim 9 further recites “a demultiplexer part separately providing the time-divided pixel signals received from the digital-analog converter to output channels of the demultiplexer corresponding to the data lines, respectively during the first half of a horizontal period and during the second half of the horizontal period.” Applicants submit that claim 9 is allowable over the cited references for the additional reason that Cairns1, Cairns2, Enami, and Nitta, analyzed singly or in any combination, do not teach or this combination of features recited by claim 9.

Claims 11, 12, and 14-29 depend from claim 9 and include by reference all of the features recited in claim 9. Applicants submit that claims 11, 12, are 14-29 allowable over the cited references at least based on their dependencies and for the same reasons given for claim 9.

Claims 35-47 each recites a data driving method for a liquid crystal display device having a combination of features including “performing a time-division on a digital pixel data and providing the time-divided digital pixel data for a horizontal period through a positive polarity output channel and a negative polarity output channel; converting the time-divided digital pixel data from the positive and negative polarity output channels into analog pixel signals having a polarity corresponding to the polarity of each of the output channels; [and] demultiplexing the time-divided positive and negative analog pixel signals to a plurality of paths corresponding to data lines.” Applicants submit that the cited references including Cairns1, Cairns2, Enami, and Nitta, analyzed singly or in combination do not teach at least this combination of features recited in claim 35. Accordingly, Applicants respectfully submit that claims 35-47 are each allowable over Cairns1, Cairns2, Enami, and Nitta for at least this reason.

Applicants believe application is in condition for allowance in light of the foregoing amendments and remarks and early, favorable action is respectfully solicited.

If for any reason the Examiner finds the application other than in condition for allowance, the Examiner is requested to call the undersigned attorney at (202) 496-7500 to discuss the steps necessary for placing the application in condition for allowance. All correspondence should continue to be sent to the below-listed address.

If these papers are not considered timely filed by the Patent and Trademark Office, then a petition is hereby made under 37 C.F.R. § 1.136, and any additional fees required under 37 C.F.R. § 1.136 for any necessary extension of time, or any other fees required to complete the

filing of this response, may be charged to Deposit Account No. 50-0911. Please credit any overpayment to deposit Account No. 50-0911. *A duplicate copy of this sheet is enclosed.*

Respectfully submitted,

Dated: February 15, 2008

By Valerie P. Hayes
Valerie P. Hayes
Registration No. **53,005**
McKENNA LONG & ALDRIDGE LLP
1900 K Street, N.W.
Washington, DC 20006
(202) 496-7500
Attorneys for Applicants